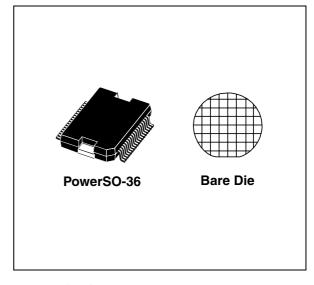


## Intelligent quad (2x5A/2x2.5A) low-side switch

#### **Features**

- Quad low-side switch
- 2 x 5A designed as conventional switch
- 2 x 2.5A designed as switched currentregulator
- Low ON resistance 2 x  $0.2\Omega$ , 2 x  $0.35\Omega$  (typ.)
- Power SO-36 package with integrated cooling area
- Integrated free wheeling and clamping Z diodes
- Output slope control
- Short circuit protection
- Selective overtemperature shutdown
- Open load detection
- Ground and supply loss detection
- External clock control
- Recirculation control
- Regulator drift detection
- Regulator error control
- Regulator resolution 5mA
- Status monitoring
- Status push-pull stages
- Electrostatic discharge (ESD) protection



### **Description**

The L9347 is an integrated quad low-side power switch to drive inductive loads like valves used in ABS systems. Two of the four channels are current regulators with current range from 250mA to 2.25A and an accuracy of 10%.

All channels are protected against fail functions. They are monitored by a status output.

Table 1.	Device	summary
----------	--------	---------

Part number	Package Packing	
L9347LF	PowerSO-36	Tray
L9347LF-TR	PowerSO-36	Tape and reel
L9347DIE1	Bare die	Bare die

Contents L9347

## **Contents**

1	Bloc	k diagram and pin connections	5
2	Elec	trical specifications	8
3	Fund	ctional Description1	3
	3.1	Overview	13
	3.2	Input circuits	13
	3.3	Output stages (not regulated) Channel 1 and 2	13
	3.4	Current regulator stages Channel 3 and 4	13
	3.5	Protective circuits	15
	3.6	Error detection	15
	3.7	Drift detection (regulated channels only)	17
	3.8	Other test modes	17
	3.9	Diagnostic table	18
4	Timi	ng diagrams 2	20
	4.1	Non regulated channels	20
	4.2	Regulated channels	23
5	Pack	kage information	27
6	Revi	sion history	28

L9347 List of tables

## List of tables

Table 1.	Device summary	. 1
Table 2.	Pin description	. 6
Table 3.	Electrical characteristcs	. 8
Table 4.	Absolute maximum ratings	10
Table 5.	Thermal data	11
Table 6.	Operating range	11
Table 7.	Detected errors	16
Table 8.	Special test mode functionality	18
Table 9.	Diagnostic table	18
Table 10.	Document revision history	28

List of figures L9347

# **List of figures**

Figure 1.	Block diagram	5
Figure 2.	Pin connections	6
Figure 3.	Input PWM to output current range	<b>1</b> 4
Figure 4.	Current accuracy according to the input and clock frequency ratio	14
Figure 5.	Output slope, resistive load	20
Figure 6.	Overload switch OFF delay	20
Figure 7.	Normal condition, resistive load, pulsed input signal	21
Figure 8.	Current overload	21
Figure 9.	Under current condition	22
Figure 10.	Open load condition in the case of pulsed input signal	22
Figure 11.	Pulsed open load conditions (regulated and non-regulated channels)	23
Figure 12.	Normal condition, inductive load	23
Figure 13.	Current overload	24
Figure 14.	Recirculation error	
Figure 15.	Current regulation error (e.g. as a result of voltage reduction)	25
Figure 16.	Over temperature	
Figure 17.	Test mode 4 (VEN low)	
Eiguro 10	PowerSO 26 mechanical data and package dimensions	

## 1 Block diagram and pin connections

Figure 1. **Block diagram** ٧S VDD VCC Internal Supply ΕN Overtemperature Channel 1 Overtemperature Channel 4 CLK Open Load Overload IN1 Q1 LOGIC ST1 GND-det. Open Load IN4 LOGIC Overload Q4 & DA ST4 IPD GND-det. Overtemperature Channel 2 Overtemperature Channel 3 Open Load Overload IN2 Q2 LOGIC ST2 GND-det. Open Load Overload IN3 LOGIC Q3 & DA ST3 IPD GND-det. drift-det. TEST

477

99AT0059

Figure 2. Pin connections

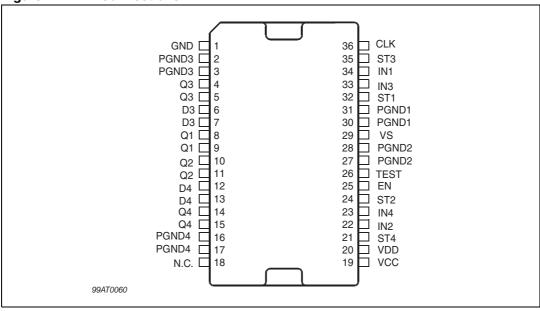


Table 2. Pin description

N°	Pin	Function	
1	GND	Logic Ground	
2, 3	PGND 3	Power Ground Channel 3	
4, 5	Q 3	Power Output Channel 3	
6, 7	D 3	Free-Wheeling Diode Channel 3	
8, 9	Q 1	Power Output Channel 1	
10, 11	Q 2	Power Output Channel 2	
12, 13	D 4	Free-Wheeling Diode Channel 4	
14, 15	Q 4	Power Output Channel 4	
16, 17	PGND 4	Power Ground Channel 4	
18	NC	Not Connected	
19	VCC	5V Supply	
20	VDD	5V Supply	
21	ST 4	Status Output Channel 4	
22	IN 2	Control Input Channel 2	
23	IN 4	Control Input Channel 4	
24	ST 2	Status Output Channel 2	
25	EN	Enable Input for all four Channels	
26	TEST	Enable Input for Drift detection	
27, 28	PGND 2	Power Ground Channel 2	
29	VS	Supply Voltage	

Table 2. Pin description (continued)

N°	Pin	Function
30, 31	PGND 1	Power Ground Channel 1
32	ST 1	Status Output Channel 1
33	IN 3	Control Input Channel 3
34	IN 1	Control Input Channel 1
35	ST 3	Status Output Channel 3
36	CLK	Clock Input

# 2 Electrical specifications

Table 3. Electrical characteristcs: (Vs = 4.8 to 18V;  $T_i$  = -40 to 150°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
Power supp	ly	L	ļ			
I <sub>SON</sub>	Supply current	$V_S \le 18V$ (outputs ON)			5	mA
I <sub>SOFF</sub>	Quiescent current	$V_S \le 18V$ (outputs OFF)			5	mA
I <sub>cc</sub>	Supply current VCC (analog supply)	VCC =5V			5	mA
I <sub>dd</sub>	Supply current VDD (digital supply)	VDD =5V f <sub>CLK</sub> =0Hz			5	uA
I <sub>dd</sub>	Supply current VDD (digital supply)	VDD =5V f <sub>CLK</sub> =250kHz			5	mA
General dia	gnostic functions		-	•		
$V_{QU}$	Open load voltage	$V_S \ge 6.5V$ (outputs OFF)	0.3	0.33	0.36	x V <sub>Q</sub>
V <sub>thGND</sub>	Signal-GND-loss threshold	VCC= 5V	0.1		1	V
V <sub>thPGL</sub>	Power-GND-loss threshold	VCC= 5V	1.5	2.5	3.5	V
f <sub>CLK,min</sub>	Clock frequency error		10		100	kHz
DC <sub>CLKe_low</sub>	Clock duty cycle error detection low	f <sub>CLK</sub> = 250 kHz		33,3	45	%
DC <sub>CLKe_high</sub>	Clock duty cycle error detection high	f <sub>CLK</sub> = 250 kHz	55	66,6		%
VS <sub>loss</sub>	Supply detection	VCC = VDD = 5V	2		4.5	V
Additional d	liagnostic functions channel 1 and c	hannel 2 (non regulated chan	nels)			
I <sub>QU1,2</sub>	Open-load current channel 1, 2	$V_S \ge 6.5V$	50		140	mA
I <sub>QO1,2</sub>	Over-load current channel 1, 2	V <sub>S</sub> ≥ 6.5V	5	7.5	9	Α
Additional d	liagnostic functions channel 3 and c	hannel 4 (regulated channels	)	I		
DC <sub>OUT</sub>	Output duty cycle range	filtered with 10ms	10		90	%
I <sub>QO3,4</sub>	Overload current channel 3,4	V <sub>S</sub> ≥ 6.5V	2.5	5	8	Α
V <sub>rerr</sub>	Recirculation error shutdown threshold (open D3/D4)	lout > 50mA	45	50	60	٧
PWM <sub>dOUT</sub>	Output PWM ratio during drift comparison	$V_{IN3} = V_{IN4} = PWM_{IN}$ $V_{TEST} = H$	-14.3		+14.3	%
Digital input	ts (IN1 to IN4, ENA, CLK, TEST). The	valid PWM-Ratio for IN3/IN4 i	s 10% to	90%		
V <sub>IL</sub>	Input low voltage		-0.3		1	V
V <sub>IH</sub>	Input high voltage		2		6	V
V <sub>IHy</sub>	Input voltage hysteresis (1)		20		500	mV

Table 3. Electrical characteristcs: (continued) (Vs = 4.8 to 18V;  $T_j$  = -40 to 150°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
I <sub>I</sub>	Input pull down current	$V_{IN} = 5V$ , $V_S \ge 6.5V$	8	20	40	μА
Digital outp	uts (ST1 to ST4)	,	•	•		
V <sub>STL</sub>	Status output voltage in low state (2)	$I_{ST} \le 40 \mu A$	0		0.4	V
M	Chatus autout valtage in high state (2)	$I_{ST} \ge -40 \mu A$	2.5		3.45	V
$V_{STH}$	Status output voltage in high state (2)	I <sub>ST</sub> ≥ -120μA	2		3.45	V
R <sub>DIAGL</sub>	R <sub>OUT</sub> + R <sub>DSON</sub> in low state		0.3	0.64	1.5	kΩ
R <sub>DIAGH</sub>	R <sub>OUT</sub> + R <sub>DSON</sub> in high state		1.5	3.2	7.0	kΩ
Power outp	uts (Q1 to Q4)					
R <sub>DSON1,2</sub>	Static drain-source ON-resistance Q1 and Q2 (non-reg. channels)	$\begin{split} &I_Q = 1A; \ V_S \ge 9.5V \\ &T_j = 25^{\circ}C \\ &T_j = 125^{\circ}C^{(3)} \\ &T_j = 150^{\circ}C^{(4)} \end{split}$		0.2	0.5 0.5	W W W
R <sub>DSON3,4</sub>	Static drain-source ON-resistance Q3 and Q4 (reg. channels)	$\begin{split} I_Q &= 1\text{A}; \ V_S \ge 9.5\text{V} \\ T_j &= 25^{\circ}\text{C} \\ T_j &= 125^{\circ}\text{C} \stackrel{(3)}{=} \\ T_j &= 150^{\circ}\text{C} \stackrel{(4)}{=} \end{split}$		0.35	0.75 0.75	Ω Ω Ω
V <sub>F_250mA</sub>	Forward voltage of free wheeling path D3, D4 @250mA	I <sub>D3/4</sub> = -250mA	0.5		1.5	V
V <sub>F_2.25A</sub>	Forward voltage of free wheeling path D3, D4 @2.25A	I <sub>D3/4</sub> = -2.25A	2.0		4.5	V
R <sub>sens</sub>	Sense resistor = $(V_{F_2.25A}$ $V_{F_250mA})/2A$			1		Ω
V <sub>Z</sub>	Z-diode clamping voltage	$I_Q \ge 100 mA$	45		60	V
I <sub>PD</sub>	Output pull down current	V <sub>EN</sub> = H, V <sub>IN</sub> = L	10		150	μА
I <sub>Qlk</sub>	Output leakage current	V <sub>EN</sub> = L; V <sub>Q</sub> = 20V			5	μА
Timing						
t <sub>ON</sub>	Output ON delay time	I <sub>Q</sub> = 1A	0	5	20	μS
t <sub>OFF</sub>	Output OFF delay time channel	I <sub>Q</sub> = 1A	0	10	30	μS
toffreg	Output OFF delay time regulator	(5)		528		μS
t <sub>r</sub>	Output rise time	I <sub>Q</sub> = 1A	0.5	1.5	8	μS
t <sub>f</sub>	Output fall time	I <sub>Q</sub> = 1A	0.5	1.5	8	μS
t <sub>sf</sub>	Short error detection filter time	f <sub>CLK</sub> = 250kHz DC = 50% <sup>(5)</sup>	4		8	μS
t <sub>lf</sub>	Long error detection filter time	f <sub>CLK</sub> = 250kHz DC = 50% <sup>(5)</sup>	16		32	μS
t <sub>SCP</sub>	Short circuit switch-OFF delay time	(5)	4		30	μS

 Table 3.
 Electrical characteristcs: (continued)

(Vs = 4.8 to 18V;  $T_i$  = -40 to 150°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
t <sub>D</sub>	Status delay time	(5)	896		1024	us
t <sub>RE</sub>	Regulation error status delay time	(5) (reg. channels only)		10		ms
t <sub>Dreg</sub>	Output off status delay time	(5) (reg. channels only		528		μS
Reg. curren	Reg. current accuracy (reg. channels only)					
I <sub>Q3/Q4</sub>	Minimum current	DC = 10%	200	250	300	mA
I <sub>Q3/Q4</sub>	Maximum current	DC = 90%	2	2.25	2.5	Α
I <sub>REG</sub>	Max. regulation deviation @ DC 10% - 90%	$250\text{mA} < I_{Q3/Q4} < 400\text{mA} \\ 400\text{mA} \le I_{Q3/Q4} \le 800\text{mA} \\ 800\text{mA} < I_{Q3/Q4} < 2.25\text{A}$			±10 ±6 ±10	% %
Δl <sub>Q3/Q4</sub>	Min. quant. step			5		mA
Frequencies	S					
	CLK frequency	crystal-controlled		250		kHz
	Input PWM frequency	(reg. channels only)		2		kHz

<sup>1.</sup> This parameter will not be tested but assured by design

- 3. Measured chip, bond wires not included
- 4. Measured on Power SO-36 devices
- 5. Digital filtered with external clock, only functional test

Table 4. Absolute maximum ratings

The absolute maximum ratings are the limiting values for this device. Damage may occur if this device is subjected to conditions which are beyond these values

Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
EQ	Switch off energy for inductive loads				50	mJ
Voltages						
V <sub>S</sub>	Supply voltage		-0.3		40	V
V <sub>CC</sub> , V <sub>DD</sub>	Supply voltage		-0.3		6	V
V <sub>Q</sub>	Output voltage static				40	V
$V_{Q}$	Output voltage during clamping	t < 1ms			60	V
$V_{IN}, V_{EN}$	Input voltage IN1 to IN4, EN	I <sub>I</sub> < I10ImA	-1.5		6	٧
V <sub>CLK</sub>	Input Voltage CLK		-1.5		6	V
V <sub>ST</sub>	Output voltage status		-0.3		6	V
$V_D$	Recirculation circuits D3, D4				40	٧
V <sub>DRmax</sub>	max. reverse breakdown voltage of free wheeling diodes D3, D4				55	V

<sup>2.</sup> Short circuit between two digital outputs (one in high the other in low state) will lead to the defined result "LOW"

Table 4. Absolute maximum ratings (continued)

The absolute maximum ratings are the limiting values for this device. Damage may occur if this device is subjected to conditions which are beyond these values

Symbol	Parameter	Test conditions	Min	Тур	Max	Unit		
Currents	Currents							
I <sub>Q1/2</sub>	Output current for Q1 and Q2		>5		internal limited	Α		
I <sub>Q3/4</sub>	Output current for Q3 and Q4		>3		internal limited	Α		
I <sub>Q1/2</sub> , I <sub>PGND1/2</sub>	Output current at reversal supply for Q1 and Q2		-4			Α		
I <sub>Q3/4</sub> , I <sub>PGND3/4</sub>	Output current at reversal supply for Q3 and Q4		-2			Α		
I <sub>ST</sub>	Output current status pin		-5		5	mA		
ESD Protect	ESD Protection							
ESD	Electrostatical Discharging	MIL883C	±2			kV		
ESD	Output Pins (Qx, Dx)	vs. Common GND (PGND1-4 + GND)	<u>±</u> 4			kV		

Table 5. Thermal data

Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
T <sub>j</sub>	Junction temperature	T <sub>j</sub>	-40		150	°C
T <sub>jc</sub>	Junction temperature during clamping (life time)	$\Sigma t = 30min$ $\Sigma t = 15min$			175 190	°C
T <sub>stg</sub>	Storage temperature	T <sub>stg</sub>	-55		150	°C
T <sub>th</sub>	Overtemperature shutdown threshold	(1)	175		200	°C
T <sub>hy</sub>	Overtemperature shutdown hysteresis	(1)		10		°C
R <sub>thJC</sub>	Thermal resistance junction to case	R <sub>thJC</sub>			2	K/W

<sup>1.</sup> This parameter will not be tested but assured by design.

Table 6. Operating range

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>S</sub>	Supply voltage		4.8		18	V
$V_{CC}$ , $V_{DD}$	Supply voltage		4.5		5.5	٧
dV <sub>S</sub> /dt	Supply voltage transient time		-1		1	V/μs
V <sub>Q</sub>	Output voltage static		-0.3		40	V
V <sub>Q</sub>	Output voltage induced by inductive switching	Voltage will be limited by internal Z-diode clamping			60	V
V <sub>ST</sub>	Output voltage status		-0.3		6	V

Table 6. Operating range (continued)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>ST</sub>	Output current status		-1		1	mA
T <sub>j</sub>	Junction temperature		-40		150	°C
T <sub>jc</sub>	Junction temperature during clamping	$\Sigma = 30$ min $\Sigma = 15$ min			175 190	°C

### 3 Functional Description

#### 3.1 Overview

The L9347 is designed to drive inductive loads (relays, electromagnetic valves) in low side configuration. Integrated active Zener-clamp (for channel1 and 2) or free wheeling diodes (for channel 3 and 4) allow the recirculation of the inductive loads. All four channels are monitored with a status output. All wiring to the loads and supply pins of the device are controlled. The device is self-protected against short circuit at the outputs and overtemperature. For each channel one independent push-pull status output is used for a parallel diagnostic function.

Channel 3 and 4 work as current regulator. A PWM signal on the input defines the target output current. The output current is controlled through the output PWM of the power stage. The regulator limits of 10% or 90% are detected and monitored with the status signal. The current is measured during recirculation phase of the load.

A test mode compares the differences between the two regulators. This "drift" test compares the output PWM of the regulators. By this feature a drift of the load during lifetime can be detected.

### 3.2 Input circuits

The INput, CLK, TEST and ENable inputs, are active high, consist of Schmidt triggers with hysteresis. All inputs are connected to pull-down current sources.

### 3.3 Output stages (not regulated) Channel 1 and 2

The two power outputs (5A) consist of DMOS power transistors with open drain output. The output stages are protected against short circuit. Via integrated Zener clamp diodes the overvoltage of the inductive loads due to recirculation are clamped to typ. 52V for fast shut off of the valves. Parallel to the DMOS transistors there are internal pull-down current sources. They are provided to assure an open load condition in the OFF state. With EN=low this current source is switched off, but the open load comparator is still active.

### 3.4 Current regulator stages Channel 3 and 4

The current-regulator channels are designed to drive inductive loads. The target value of the current is given by the duty cycle (DC) of the 2kHz PWM input signal. The following figure shows the relation between the input PWM and the output current and the specified accuracy.

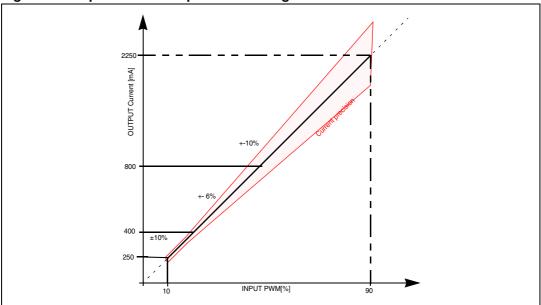


Figure 3. Input PWM to output current range

The ON period of the input signal is measured with a 1MHz clock, synchronized with the external 250kHz clock. For requested precision of the output current the ratio between the frequencies of the input signal and the external 250kHz clock has to be fixed according to the graph shown in *Figure 3*.

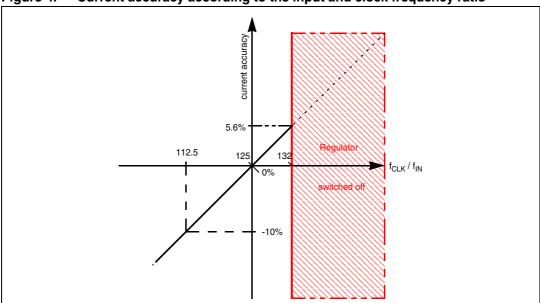


Figure 4. Current accuracy according to the input and clock frequency ratio

The theoretical error is zero for  $f_{CLK}$  /  $f_{IN}$  = 125.

If the period of the input signal is longer than 132 times the period of the clock the regulator is switched off. For a clock frequency lower than 100kHz the clock control will also disable the regulator. For high precision applications the clock frequency and the input frequency have to be correlated.

The output current is measured during the recirculation of the load. The current sense resistor is in series to the free wheeling diode. If this recirculation path is interrupted the regulator stops immediately and the status output remains low for the rest of the input cycle.

The output period is 64 times the clock period. With a clock frequency of 250kHz the output PWM frequency is 3.9kHz. The output PWM is synchronized with the first negative edge of the input signal. After that the output and the input are asynchronous. The first period is used to measure the current. This means the first turn-on of the power is  $256\mu s$  after the first negative edge of the input signal.

As regulator a digital PI-regulator with the Transfer function for:

KI: and KP: 0.96

for a sampling time of 256µs is realised.

To speed up the current settling time the regulator output is locked to 90% output PWM untill the target current value is reached. This happens alsowhen the target current value changes and the output PWM reaches 90% during the regulation. The status output gets low if the target current value is not reached within the regulation error delay time of  $t_{\rm RE}$ =10ms. The output PWM is than out of the regulation range from 10% to 90%.

#### 3.5 Protective circuits

The outputs are protected against current overload, overtemperature, and power-GND-loss. The external clock is monitored by a clock watchdog. This clock watchdog detects a minimal frequency f<sub>CLK,min</sub> and wrong clock duty cycles. The allowed clock duty cycle range is 45% to 55%. The current-regulator stages are protected against recirculation errors, when D3 or D4 is not connected. All these error conditions shut off the power stage and invert the status output information.

#### 3.6 Error detection

The status outputs indicate the switching state under normal conditions (status LOW = OFF; status HIGH = ON). If an error occurs, the logic level of the status output is inverted, as listed in the diagnostic table below. All external errors, for example open load, are filtered internally. The following table shows the detected errors, the filter times and the detection mode (on/off).

Table 7. Detected errors

	ON State EN &IN = HIGH	OFF State EN &IN = LOW	Filter time	Reset done by		
Short circuit of the load	Х		t <sub>sf</sub>	EN & IN = "LOW" for $T_D$ or $T_{Dreg}$		
Open load (under voltage detection)		Х	t <sub>lf</sub>	timer T <sub>D</sub>		
Open load (under current detection)	Х		t <sub>sf</sub>	timer T <sub>D</sub>		
Over temperature	Х		t <sub>sf</sub>	EN & IN = "LOW" for $T_D$ or $T_{Dreg}$		
Power-GND-loss	х	х	t <sub>lf</sub>	in on: EN & IN = "LOW" for $T_D$ or $T_{Dreg}$ in off: timer $T_D$		
Signal-GND-loss	Х	Х	t <sub>lf</sub>	timer T <sub>D</sub>		
Supply-VS-loss	Х	Х	t <sub>lf</sub>	timer T <sub>D</sub>		
Clock control	х	Х	no	in on: EN & IN = "LOW" for $T_D$ or $T_{Dreg}$ in off: timer $T_D$		
Output voltage clamp active	X (regulated channels)		no	in on: EN & IN = "LOW for $T_D$ or $T_{Dreg}$ in off: timer $T_D$		

EN&IN=low means that at least one between enable and input is low. For the inputs IN = low means also no input PWM. For the regulator input period longer than  $T_{Dreg}$  and for the standard channel input period longer than  $T_{Dreg}$ .

A detected error is stored in an error register. The reset of this register is made with a timer  $T_D$ . With this approach all errors are present at the status output at least for the time  $T_D$ .

All protection functions like short circuit of the output, overtemperature, clock failure or power-GND-loss in ON condition are stored into an internal "fail" register. The output is then shut off. The register must be reset with a low signal at the input. A "low signal" means that the input is low for a time longer than  $T_D$  or  $T_{DReg}$  for the reulated channel, otherwise it is interpreted as a PWM input signal and the register is left in set mode.

Signal-GND-loss and VS-loss are detected in the active on mode, but they do not set the fail register. This type of error is only delayed with the standard timer  $t_{\rm lf}$  function.

Open load is detected for all four channels in on and off state.

Open load in off condition detects the voltage on the output pin. If this voltage is below 0.33  $^{\star}$  VS the error register is set and delayed with  $T_{D\cdot}$  A sink current stage pull the output down to ground, with EN high. With EN low the output is floating in case of openload and the detection is not assured. In the ON state the load current is monitored by the non-regulated channels. If it drops below the specified threshold value  $I_{QU}$  an open load is detected and the error register is set and delayed with  $T_{D\cdot}$  A regulated channel detects the open load in the on state with the current regulator error detection. If the output PWM reaches 90% for a time longer than  $t_{RE}$  than an error occurs. This could happen when no load is connected, the

resistivity of the load is too high or the supply voltage too low. The same error is shown if the regulator is not able to reduce the current in the load in the time  $t_{RE}$ , so the output PWM falls below 10%.

A clock failure (clock loss) is detected when the frequency becomes lower than f<sub>CLK,min</sub>. All status outputs are set on error and all power outputs are shut off. The status signals remain in their state until the clock signal is present again. A clock failure during power on of VCC is detected only on the regulated channels. The status outputs of the channel 1 and 2 are low in this case.

### 3.7 Drift detection (regulated channels only)

The drift detection is used to compare the two regulated channels during regulation. This "Drift" test compares the output PWM of the regulators. The resistivity of the load influences the output PWM. The approximated formula for the output current below shows the dependency of the load resistor to the output PWM. In this formula the energy reduction during the recirculation is not taken into account. The real output PWM is higher. The testmode is enabled with IN,EN and TEST high. With an identical 2kHz PWM-Signal connected to the IN-inputs the output PWM must be in a range of +-14.3%. If the difference between the two on-times is more than  $\pm 14.3\%$  of the expected value an error is detected and monitored by the status outputs, in the same way as described above, but a drift error will not be registered and also not delayed with  $T_D$  as other errors

$$IOUT = \frac{VBAT}{RL + RON} \cdot PWM$$

**Drift Definition:** 

E.. not correlated Error of the channels

%PWM ... Corresponding ideal output PWM to a given input PWM

A 7bit output-PWM-register is used for the comparison. The register with the lower value is subtracted from the higher one. This result is multiplied by four and compared with the higher value.

#### 3.8 Other test modes

The test pin is also used to test the regulated channels in the production. With a special sequence on this pin the power stages of the regulated channels can be controlled direct from the input. No status feedback of the regulated channels is given. The status output is clocked by the regulator logic. The output sequence is a indication of a proper logic functionality. The functionality of this special test mode is shown in *Table 8*.

5/

Table 8. Special test mode functionality

EN	ln	Test	Out	Status	Note
1	Х	Х	Х	X	disable test mode
1	1	1	on	1	Drift mode
0	Х	工	off	test pattern	test condition one
0	Х	77.7.	off	test pattern	test condition two
0	Х	77.77.	off	test pattern	test condition three
0	0		off	test pattern	test condition four
0	1		on	test pattern	test condition four

For more details about the test conditions see timing diagrams in Section 4.

## 3.9 Diagnostic table

The status follows the input signal in normal operating conditions. If any error is detected the status is inverted.

Table 9. Diagnostic table

Operating Condition	Test Input TEST	Enable Input ENA	Control Input non- reg./reg. IN	Power Output/Curr ent reg. Q	Status Output ST
	L	L	L	OFF	L
Normal function	L	L	H/PWM	OFF	L
Normal function	L	Н	L	OFF	L
	L	Н	H/PWM	ON	Н
	L	L	L	OFF	Х
Open load or short to ground	L	L	H/PWM	OFF	X
Open load or short to ground	L	Н	L	OFF	Н
	L	Н	H/PWM	ON	L
Overload or short to supply	L	Н	H/PWM	OFF	L
Latched overload	L	Н	H/PWM	OFF	L
Reset latch	L	H -> L	X	OFF	L
Reset latch	L	Н	H/PWM -> L	OFF	L
Overtemperature	L	Н	H/PWM	OFF	L
Latched overtemperature	L	Н	H/PWM	OFF	L
Reset latch	L	H -> L	X	OFF	L
Reset latch	L	Н	H/PWM -> L	OFF	L
Recirculation error (reg.chn.)	L	Н	PWM	OFF	L
Latched error	L	Н	PWM	OFF	L
Reset latch	L	H -> L	X	OFF	L
Reset latch	L	Н	PWM -> L	OFF	L

Table 9. Diagnostic table (continued)

Operating Condition	Test Input TEST	Enable Input ENA	Control Input non- reg./reg. IN	Power Output/Curr ent reg. Q	Status Output ST
	L	L	L	OFF	Н
Clock failure (clock loss) (1)	L	L	H/PWM	OFF	Н
Clock failure (clock loss)	L	Н	L	OFF	Н
	L	Н	H/PWM	OFF	L
Drift <sup>(2)</sup>	Н	L	L	OFF	Х
	Н	L	H/PWM	OFF	Х
Failure	Н	Н	H/PWM	ON	L
No failure	Н	Н	H/PWM	ON	Н

<sup>1.</sup> During power on sequence only detected on channel 3 and 4 (see description).

<sup>2.</sup> This input combination is also used for an internal chip-test and must not be used.

Timing diagrams L9347

## 4 Timing diagrams

## 4.1 Non regulated channels

Figure 5. Output slope, resistive load

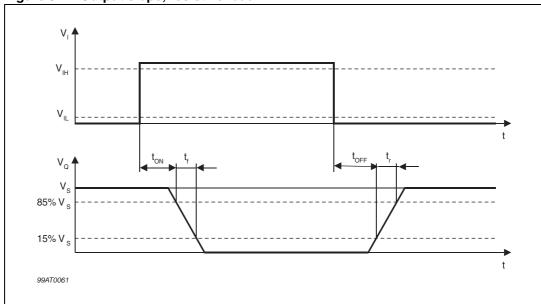
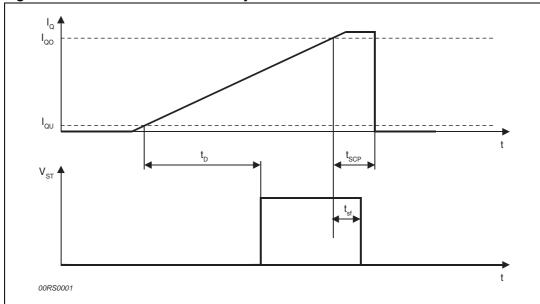


Figure 6. Overload switch OFF delay



L9347 Timing diagrams

Figure 7. Normal condition, resistive load, pulsed input signal

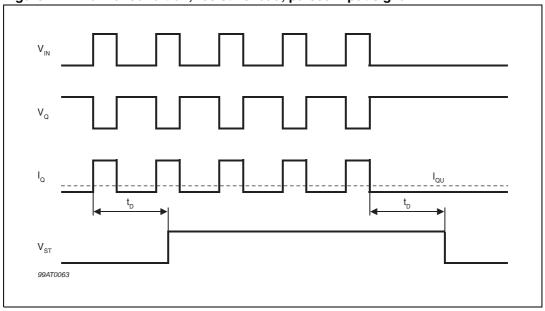
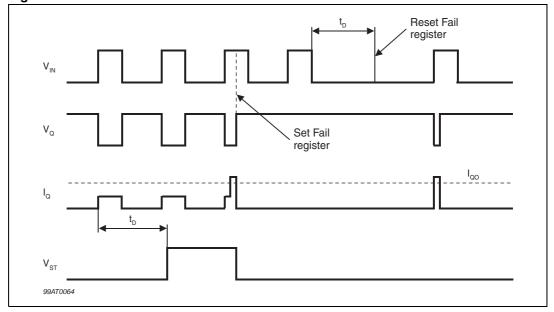


Figure 8. Current overload



Timing diagrams L9347

Figure 9 and Figure 10 show diagnostic status output at different OPEN load current conditions followed by normal operation.

Figure 9. Under current condition

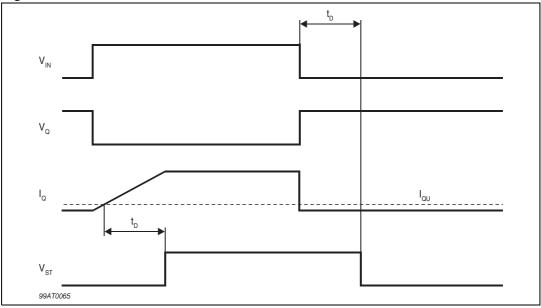
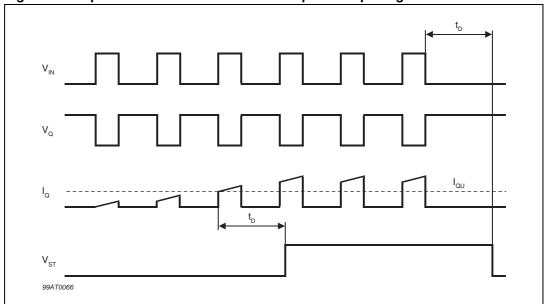


Figure 10. Open load condition in the case of pulsed input signal



**Timing diagrams** L9347

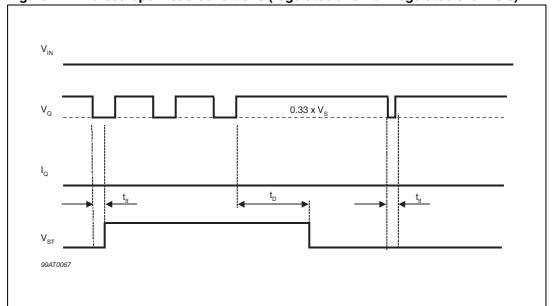
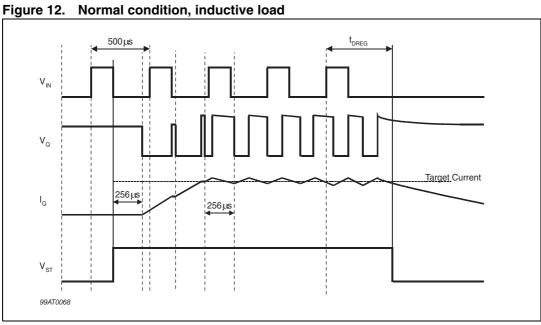


Figure 11. Pulsed open load conditions (regulated and non-regulated channels)

#### Regulated channels (timing diagrams of diagnostic with 4.2 2kHz PWM input signal)



Timing diagrams L9347

Figure 13. Current overload

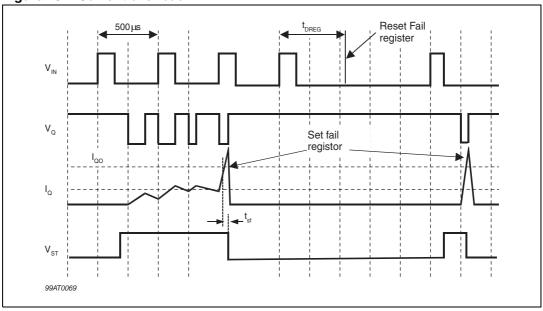
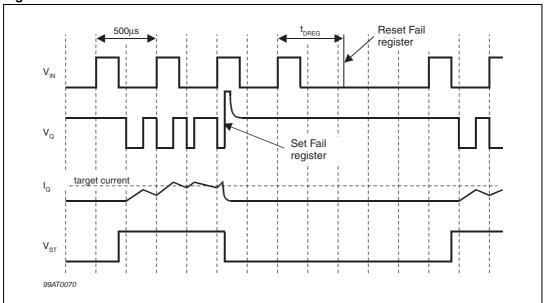


Figure 14. Recirculation error



24/29

L9347 Timing diagrams

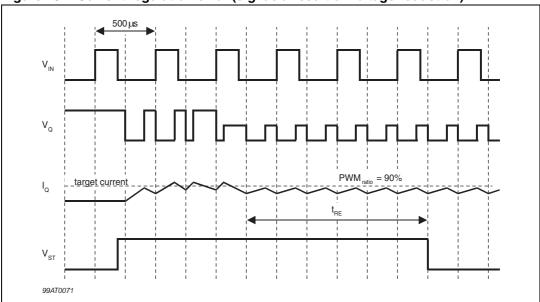
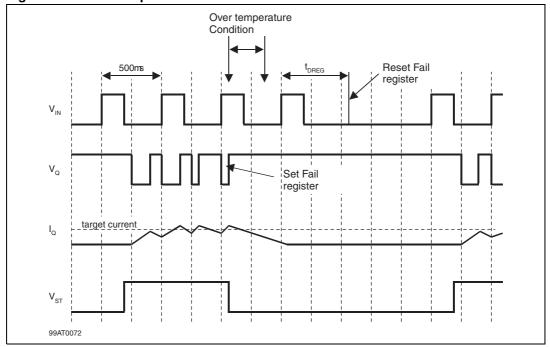
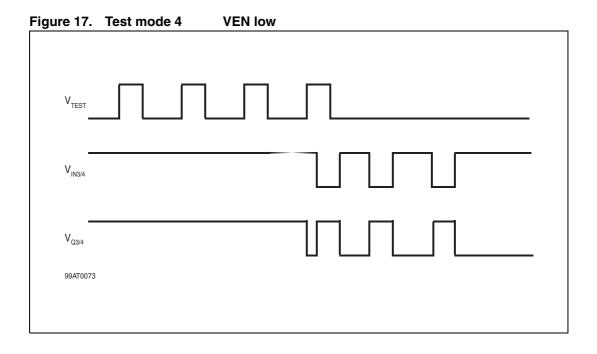


Figure 15. Current regulation error (e.g. as a result of voltage reduction)





Timing diagrams L9347

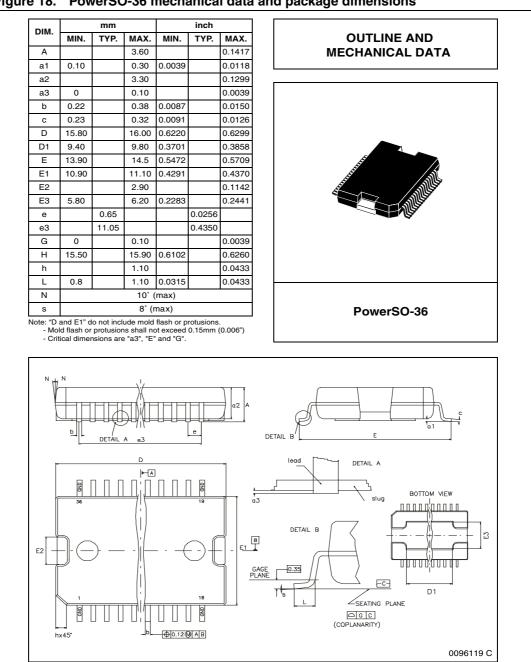


L9347 **Package information** 

#### 5 **Package information**

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 18. PowerSO-36 mechanical data and package dimensions



Revision history L9347

# 6 Revision history

Table 10. Document revision history

Date	Revision	Changes
06-July-2002	1	Initial release.
02-May-2007	2	Package change, text modifications, corporate layout changes.

#### Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2007 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

